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The role of diodes in the leakage current suppression mechanism of decoupling transformerless PV inverter topologies

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Presentation outline:

I. Introduction

II. Background & Literature review

III. The role of inverter diodes in leakage current suppression

IV. Simulation results

I. Introduction

CM voltage – Decoupling transformerless PV inverters

- **Variation of common-mode (CM) voltage generated by PWM inverters**
  - Generates ground leakage currents in grid-connected PV applications
  - Cause deterioration of the PV cells and safety hazards
- **Conventional solution: PV inverters with step-up/isolation transformers**
  - Increased cost, size, weight
- **Modern solution: Transformerless PV inverters**
  - Special structure and modulation to achieve leakage current suppression
- **Decoupling transformerless PV inverters**
  - "Decoupling" = Galvanically disconnecting the PV array from the grid during certain inverter states
  - "Zero states" = States resulting in zero inverter output voltage

Motivation – Contribution

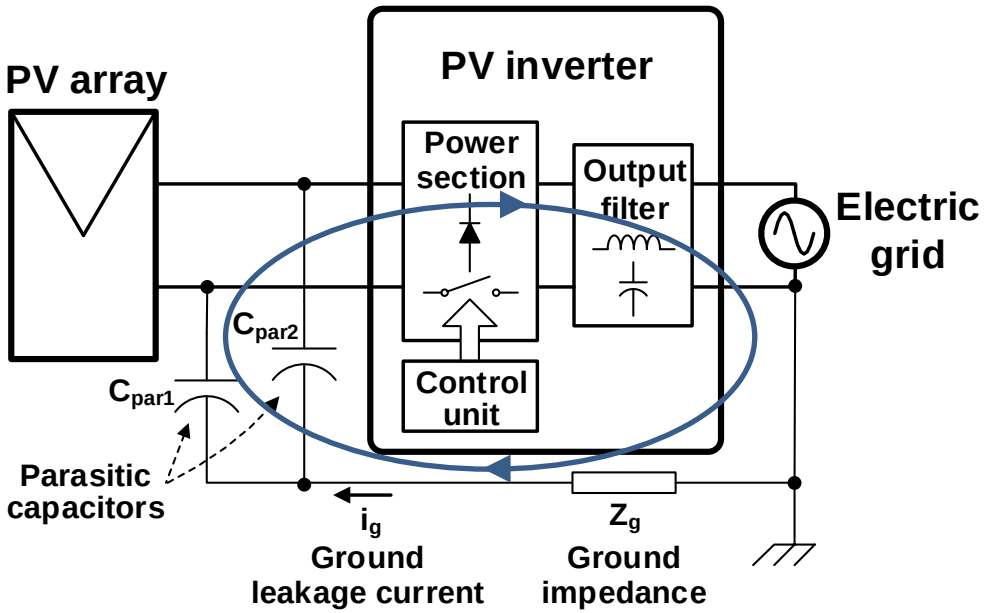
- **Galvanic disconnection between the PV array and the grid is actually not achieved at any inverter state!**
  - Inverters, apart from their semiconductor switches, include diodes, which cannot be turned off in a controlled manner.
  - The conduction routes created by these diodes cannot be interrupted, thus offering possible paths for leakage currents to flow at any moment.
- **This paper: Insight to the operation of decoupling PV inverter topologies**
  - Highlights the commonly neglected role of the inverter diodes
  - Derives the actual inverter equivalent circuit during the zero states
  - Determines the characteristics of the waveform of the inverter CM voltage
  - Aim: Expansion of the family of decoupling transformerless topologies and application of the decoupling concept to Boost and Buck-Boost PV inverters

II. Background & Literature review

CM voltage – Ground leakage current

- **CM voltage**
  - Average of the two output terminal voltages w.r.t. the negative DC-link terminal
  - Fast variation of the CM voltage gives rise to leakage currents
- **Ground leakage current path**
  - Through parasitic capacitances between the solar cells of the PV array and their grounded metal frame

$$v_{cm} = \frac{(v_a + v_b)}{2}$$



CM voltage variation

- **To avoid leakage currents, CM voltage must not vary at a high frequency**
- **Not practically possible for conventional inverter topologies**
- **Generation of PWM voltages requires transitions between different inverter states during each switching period**
- **Each state results in a different value of CM voltage**
  - Example: Conventional H-bridge inverter with **Unipolar** modulation
  - Bipolar modulation results in higher output voltage distortion

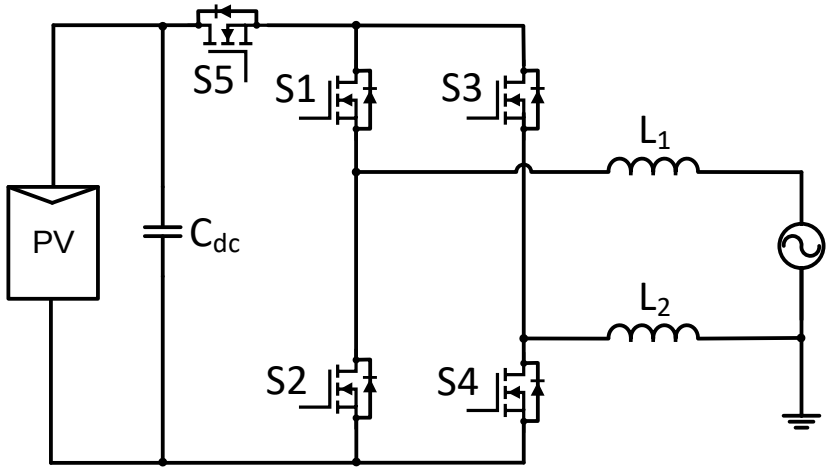
Symbol	State	v_a	v_b	v_{ab}	v_{cm}
P	10	V_{dc}	0	V_{dc}	$V_{dc}/2$
N	01	0	V_{dc}	$-V_{dc}$	$V_{dc}/2$
Z_P	11	V_{dc}	V_{dc}	0	V_{dc}
Z_N	00	0	0	0	0

Transformerless PV inverter topologies

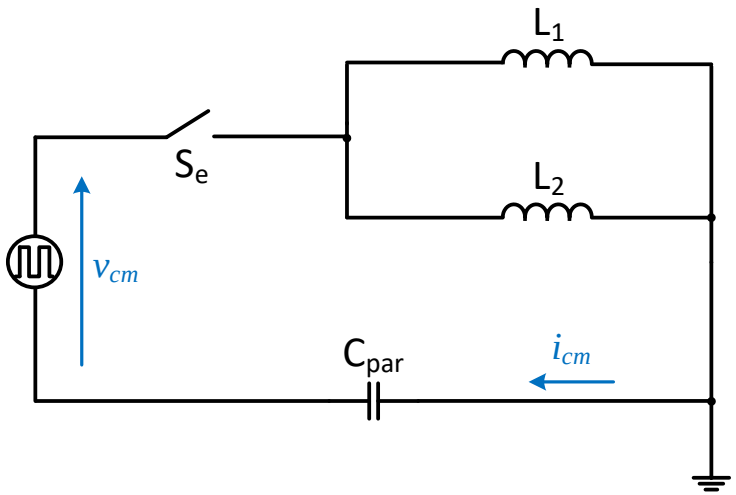
- **Modify the H-bridge structure by the addition of power semiconductor elements with the aim of enabling the use of modulation strategies that**
  - perform similarly to unipolar modulation w.r.t. output voltage quality,
  - but at the same time generate low leakage currents
- **Decoupling transformerless topologies**
  - Also referred to as zero-state isolating or decoupled topologies
  - Known to achieve leakage current suppression by disconnecting (decoupling, isolating, leaving floating) the PV array from the grid during the zero states
  - This feature is widely mentioned and reproduced in the literature

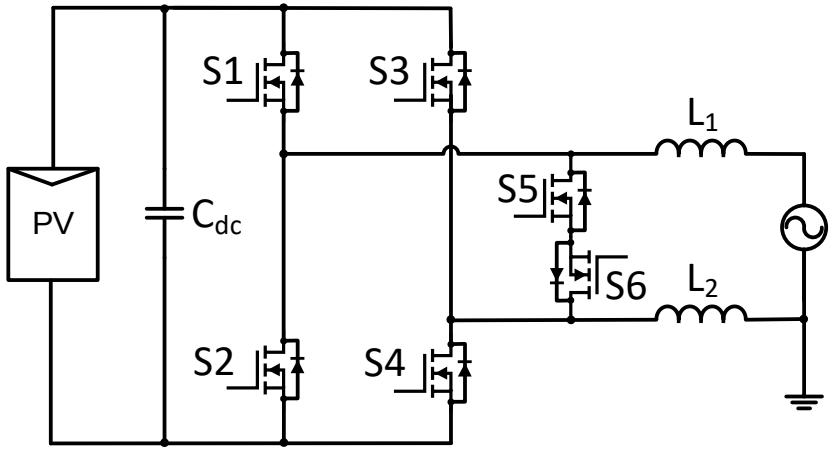
Existing decoupling topologies and equivalent circuits

- **Decoupling topologies**
  - DC decoupling: H5
  - AC decoupling: HERIC



- **Equivalent circuit**

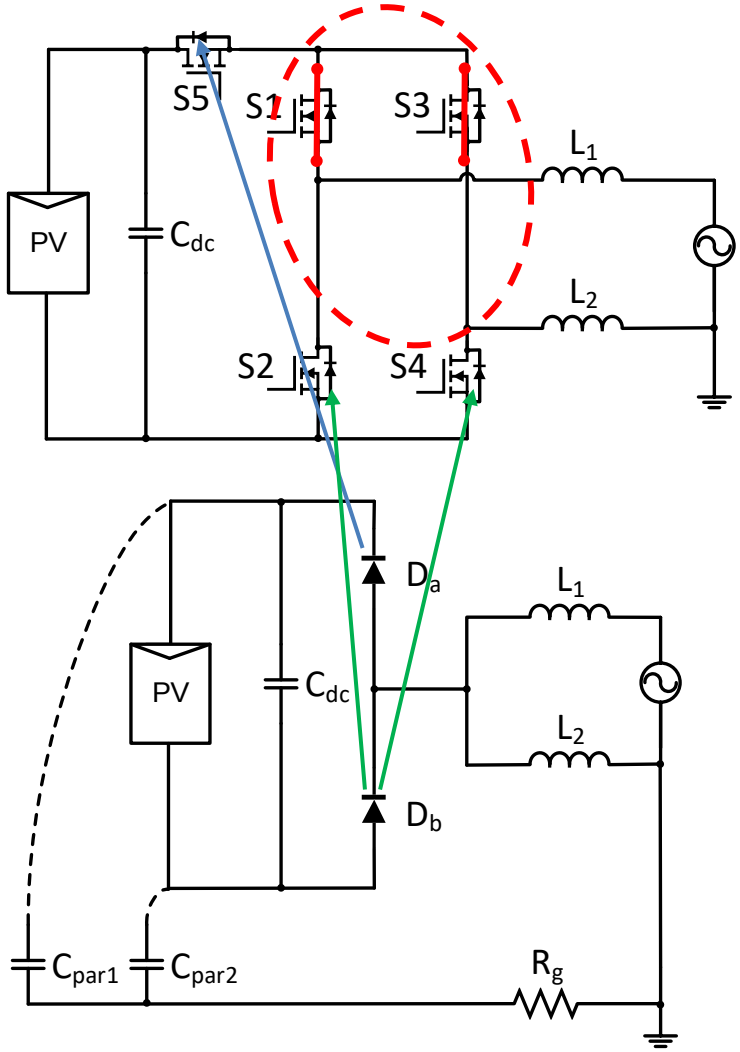




III. The role of inverter diodes

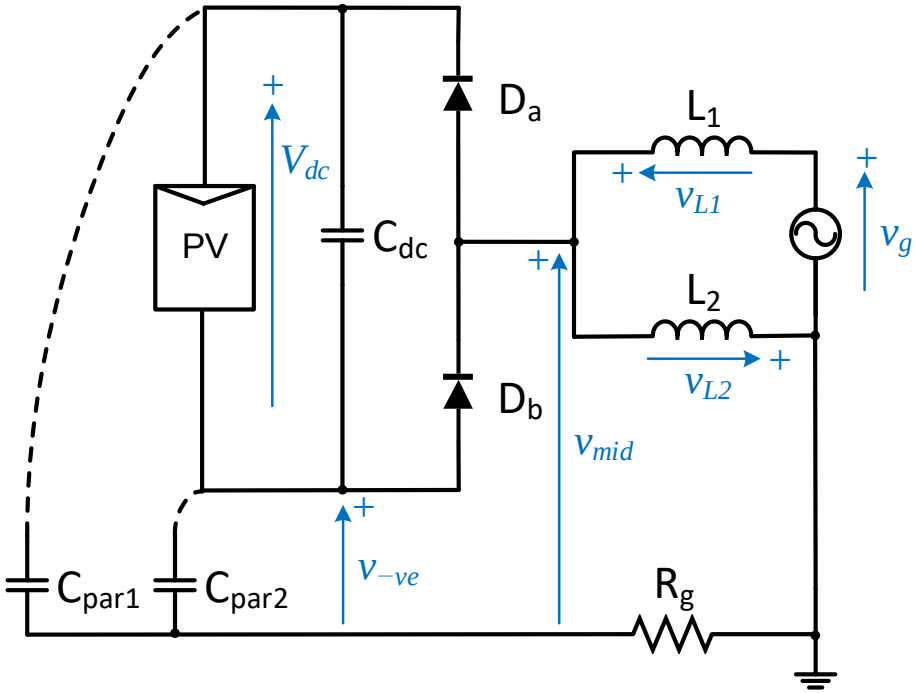
Equivalent circuit for the zero states

- Certain switches may be turned off during the zero states
- BUT their antiparallel diodes are still present and cannot be prevented from carrying current
- D_a and D_b shown in the equivalent circuit represent different inverter diodes, or parallel connection of diodes
- Example: H5 zero state
  - Only S1 and S3 are ON
  - D_a is D5, and D_b is D2 // D4



The role of inverter diodes

- **No actual decoupling of the PV array from the grid during the inverter zero states**
- **Why do the diodes not conduct?**
- **An inductive voltage divider is formed, resulting in**
  - $v_{mid} = v_g / 2$
- **It will be shown that**
  - D_a is reverse-biased because $v_{-ve} + V_{dc} > v_{mid}$
  - D_b is reverse-biased because $v_{-ve} < v_{mid}$



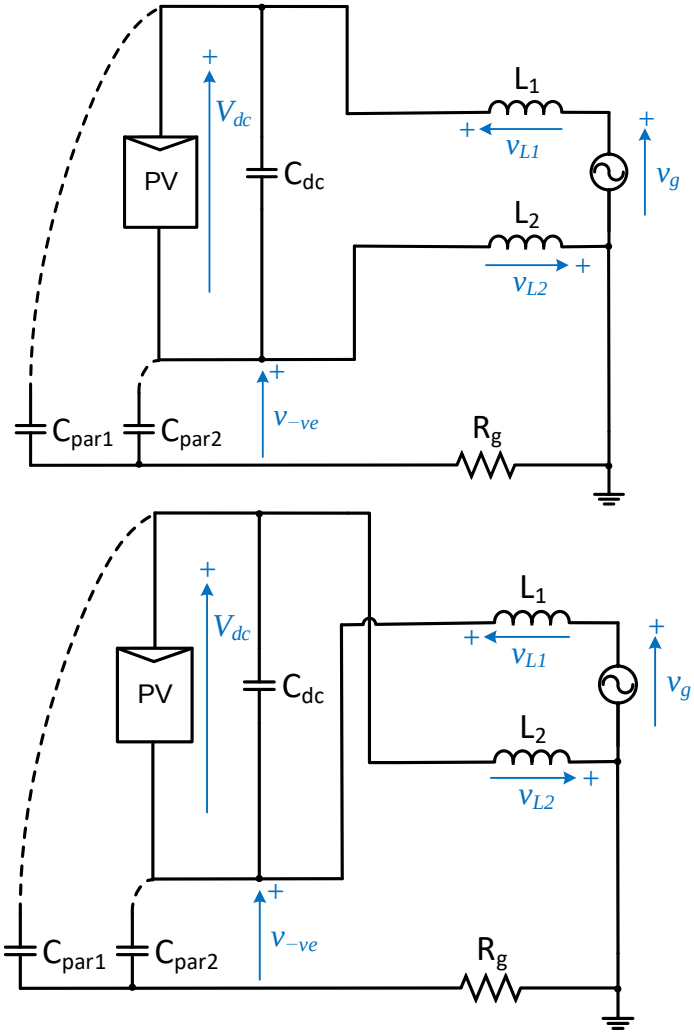
The role of inverter diodes (cont.)

- **Figures: Equivalent circuits for the P and N states**
  - From KVL, for both states, neglecting voltage drops due to CM currents:

    $v_{-ve} \approx (v_g - V_{dc}) / 2$
  - D_a is reverse-biased because

    $v_{-ve} + V_{dc} \approx (v_g + V_{dc}) / 2 > v_g / 2$
  - D_b is reverse-biased because

    $v_{-ve} \approx (v_g - V_{dc}) / 2 < v_g / 2$

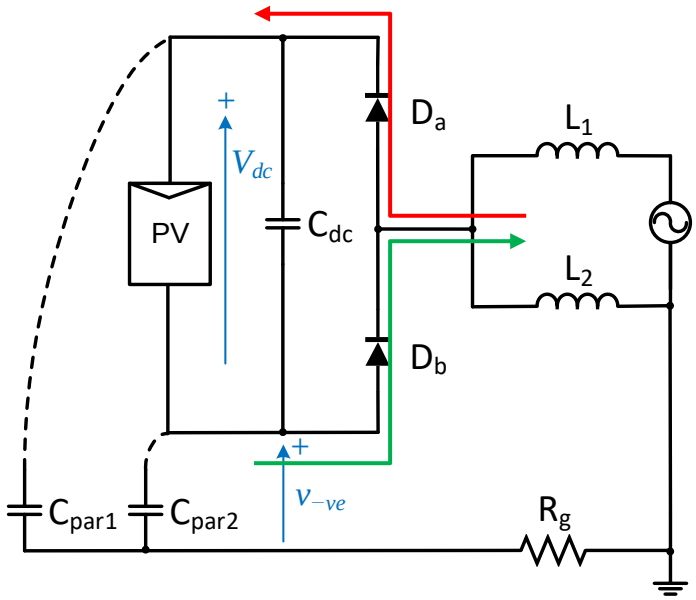


Impact on the CM voltage waveform

- **Commonly accepted statement: "CM currents flow during the P and N states, but not during the zero states"**
- **However**
  - The duration of the P and N states is typically not adequate for CM currents to charge the parasitic capacitors to the voltage levels derived earlier.
  - Especially in the areas of the inverter reference voltage zero-crossings, the duty cycles of the P and N states are so low that the deviation of the parasitic capacitor voltages from $(v_g \pm V_{dc}) / 2$ becomes evident.
- **Contradiction!**
  - The fact that the CM currents that flow during the P and N states do not last for long enough to bring the parasitic capacitor voltages to $(v_g \pm V_{dc}) / 2$, indicates that CM currents **still flow** when entering the zero states.

Impact on the CM voltage waveform (cont.)

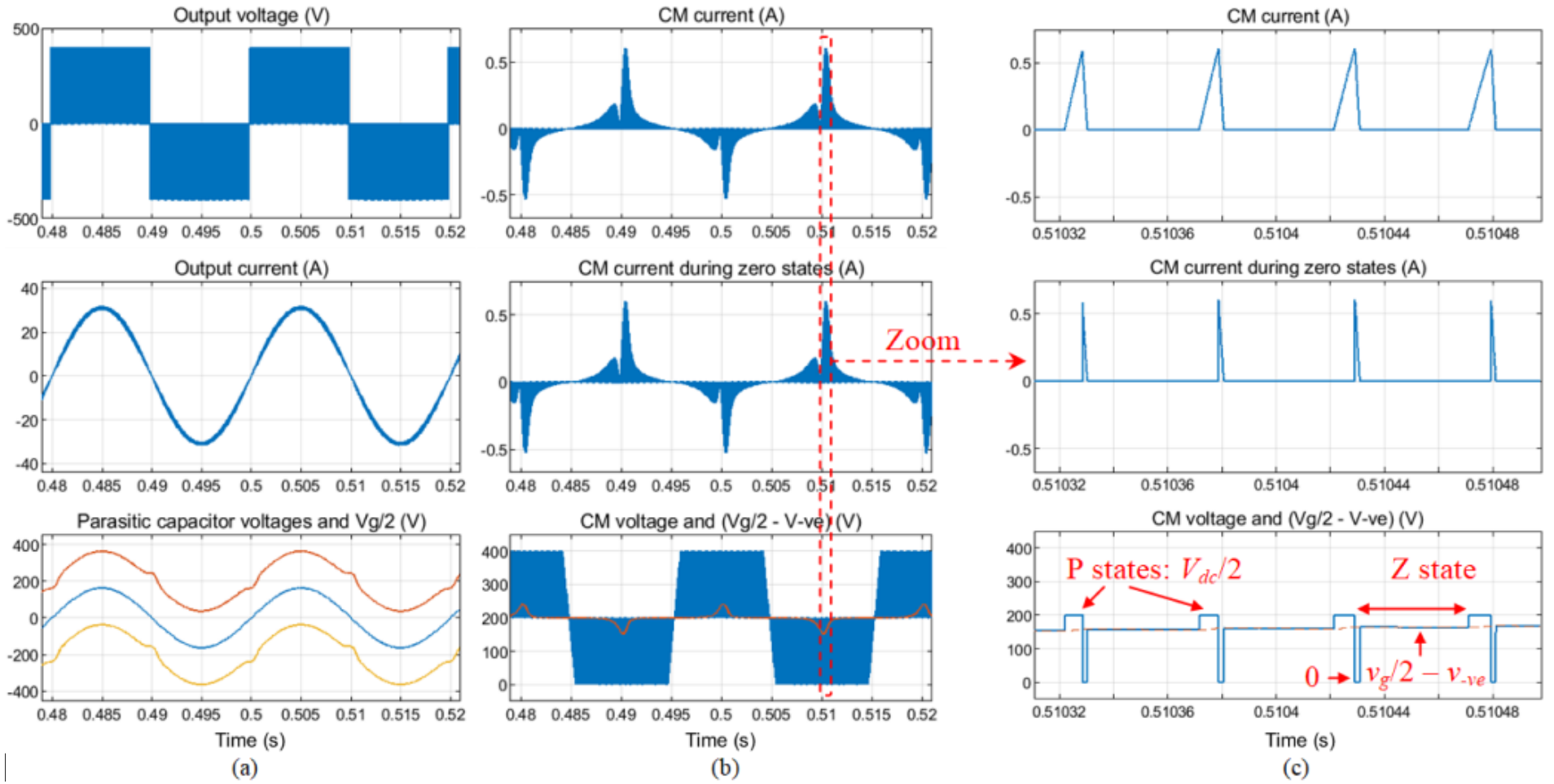
- **Actual behaviour**
  - The existence of inductors L1 and L2 in the CM current path does not allow an instantaneous drop of the CM current to zero.
  - The CM current gradually drops (free-wheels) towards zero, flowing through a current path that includes either D_a or D_b, depending on its initial direction.
  - For the duration of this drop, the CM voltage is clamped to V_{dc} if D_a is conducting, or to 0 if D_b is conducting.
  - For the remaining of each zero state, since there is no CM current flow, the CM voltage is equal to (v_g / 2 – v_{-ve}).



Simulation in MATLAB-Simulink

- **PV inverter**
  - Topology: H5 transformerless
  - Power rating: 5kVA
  - Switching frequency: 20kHz
- **PV array**
  - Simulated as a DC source with voltage V_{dc} = 400V
  - Parasitic capacitances to ground of 250nF (total of 100nF per PV array kW)
- **Filter inductors – Ground resistance**
  - L1 = L2 = 1mH
  - R_g = 1Ω

Simulation results in MATLAB-Simulink



Conclusion

- **This paper analysed the leakage current suppression mechanism of the zero-state decoupling transformerless PV inverter topologies.**
- **It demonstrated that the inverter diodes actively participate in this mechanism and affect the common-mode voltage characteristics.**
- **The final outcomes can contribute towards**
  - obtaining more accurate estimates for the generated leakage current,
  - improving modelling methods and simulation tools,
  - developing new transformerless PV inverter topologies, including Boost and Buck-Boost PV inverter topologies.

Acknowledgement

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Thank you for your attention !

Questions ?